AN EFFICIENT COST ESTIMATION MODEL OF CAD SILICON

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ABSTRACT: The costs associated with silicon design, testing, and CAD are discussed in detail in this paper. A straightforward cost model is presented to assess the potential impact of cost growth on the VLSI industry and all major factors that contribute to the rapid growth of manufacturing costs are explained.

KEYWORDS: Transistor cost, Lightly doped drain, Integrated circuits

I INTRODUCTION

Design and test, and as a result, CAD, cannot change independently of IC manufacturing trends, which provide the majority of the industry's revenue. There are numerous components in the design-manufacturing interface. Manufacturing constraints, which take the form of design rules and a variety of device characteristics, are the most obvious and well-known. The idea of silicon cost is one more significant but less obvious connection between design and manufacturing. This idea has an indirect effect on the ways in which the IC industry as a whole evolves. Multimillion transistor systems on a single die are feasible and cost-effective as a result of the constant decline in the cost of silicon, calculated per IC transistor. As a result, the cost of IC manufacturing has been viewed as relevant only for high volume production, while design, test, and CAD have focused solely on design complexity and time-to-market issues.

The perception of manufacturing costs has begun to shift over the past few years [1]. The cost of manufacturing facilities is rising at an exponential rate and is expected to soon reach one billion dollars per fabline [2,3,4]. The conditions of the market have also shifted. Expanded contest has prompted a reduction in beforehand rewarding overall revenues [5]. How will the aforementioned adjustments affect the market for microelectronics? How will the new situation on the interface between

manufacturing and design appear? What kind of adjustments to IC manufacturing and design strategies might be required? What requirements must new CAD tools and design strategies address? Before any potential negative effects of the increase in manufacturing costs occur, the design/CAD community ought to discuss these and a great number of other similar questions. The reason for this paper is to give an outline of the IC assembling cost area in request to start conversation which tends to the abovementioned concerns.

Basic facts about the electronics industry in general and microelectronics in particular can help set the stage for the discussion in this paper. The entire electronics industry has expanded over the past ten years at a rate of approximately 40 billion dollars per year in sales of electronic equipment, reaching 700 billion dollars this year [6]. Such headway has been gained conceivable by the headway of the IC business which has represented around 10-13% of the all out gadgets market size. The advancement in microelectronics, thusly, was empowered by the continually diminishing size of a typical coordinated semiconductor. Figure depicts the rate of change in transistor size, which is traditionally characterized by the minimum length of a transistor channel, also known as minimum feature Fig 1 [1,6,7,8]

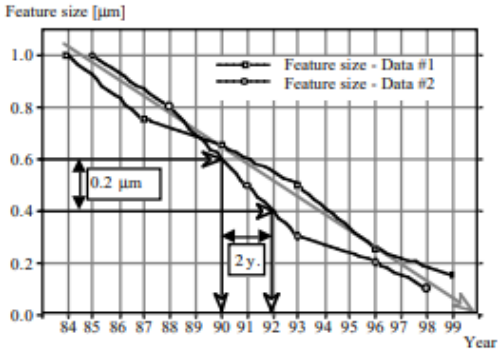

Fig. 1. Minimum feature size as a function of time.

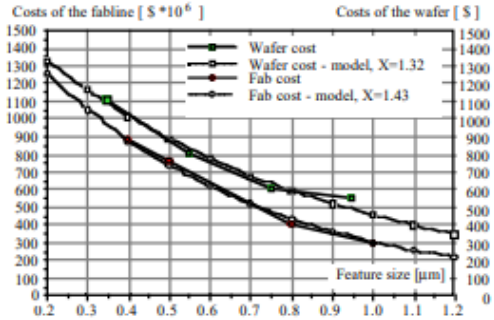

Fig. 2. Cost of a fabrication line and manufacturing wafer.

II TRANSISTOR COST ESTIMATION MODEL

Two seemingly contradictory observations emerge from the aforementioned summation. On the one hand, rapidly rising costs are caused by the complexity of the processes and manufacturing equipment. The rate of progress, on the other hand, appears to be unaffected by these rising costs. A good way to explain the above contradiction is to focus on the manufacturing cost that is calculated per transistor, which is a good way to measure

the cost of an IC's functionality. This cost has always been going down [6], making it possible to sell the new functionality at very attractive profit margins. As a result, overall increases in manufacturing costs did not really matter in the past. The situation has changed recently. There are some signs that the cost of a transistor may no longer be going down [10], or at least that the rate at which it is going down may slow down [11]. Since the reduction in transistor size may not result in gains in both performance and cost, this change may have a significant impact on the entire IC industry. This section aims to perform a cost analysis of transistors in order to: a) Determine whether established cost trends for transistors will persist into the future and b) Show the complexity of the IC manufacturing cost issue a functioning (fault-free) integrated circuit, the cost of a transistor, Ctr, can be expressed as:

$$C_{tr} = \frac{C_w}{N_{ch} N_{tr} Y} \quad (1)$$

III COST OF TRANSISTOR ESTIMATES

The constant decrease in the cost of an IC transistor has often been taken for granted. In some cases transistor cost has been even viewed as almost design/test irrelevant [27]. And such a view is understandable since in the past typical design/test objectives were focused on the IC performance only and manufacturing costs were determined through the choice of technology, design style and die size limits i.e., through arbitrary decisions which were beyond the typical design/test domain. In addition lucrative profit margins amplified the performance side of the design objectives and allowed for less cost effective design solutions. Now, as the situation may change and cost could become one of the main concerns it is necessary to re-examine the transistor's basic cost trends and to analyze the design – cost dependency.

The economic realities of memory production have a significant impact on the momentum of the entire IC industry because memories are the largest "consumers" of process and equipment research and development. However, the presented argument demonstrates that non-memory products may not benefit from what is cost-effective for memories. It is also obvious that redundancy-free integrated circuits may not be able to maintain their cost reduction of transistors under certain conditions.

As a result, the IC industry's business and technology sectors, which cannot benefit from high volume, single-product, high yield manufacturing operations, are likely to undergo significant shifts. Design-based manufacturing cost optimization is also expected to gain prominence among these changes.

IV OBJECTIVES

The primary message that has been conveyed thus far in this paper is that the rising cost of IC manufacturing needs to be "contained" and that design, test, and CAD should assist the IC industry in the upcoming cost-driven transformation. There are two fundamental reasons why this need has not been adequately met up to this point: inadequate cost models and a lack of integration between system testing and IC manufacturing goals.This point can be supported by a number of examples. The situation in the MCM arena is the best of them all.

MCMs are still viewed as a packaging domain rather than a system/IC design opportunity to save money. For instance, it is possible to demonstrate that an active silicon substrate—a very expensive substrate—can be used to construct a smart substrate system [30]. This system can reduce the overall cost of the system by self-testing and enables cost savings that are impossible with cheaper but passive substrates [31]. However, the cost of the substrate itself is the focus of traditional MCM strategies. As a result, the overall cost savings at the system level are not readily apparent, and typical MCMs are regarded as a more expensive method of packaging small and medium-sized systems.

There are numerous additional examples that clearly demonstrate that the absence of integration between design, testing, and manufacturing is, on the one hand, a cause for unneeded price increases and, on the other, a significant opportunity to save money. Take, for instance, the test. The cost and complexity of test generation can be reduced with the help of DFT and BIST techniques. However, designers are hesitant to allocate the resources (such as silicon area and/or performance) necessary to use these methods. The issue lies in the absence of an adequate method for quantifying the benefits that any BIST or DFT technique would offer in return, such as a reduction in the cost of test generation, an increase in overall test quality, or a reduction in time to market.

The fundamental issue is that system-level cost reduction is only possible with a cost modeling strategy that incorporates into a single model quantities such as: yield of the system's parts, expressed as a function of each and every strategic design variable (Ntr, for example), Cost of testing as a function of the likelihood of fault escapes is available [32] and many others.By listing the cost models that are required for overall system-level cost optimization, Figure 3 illustrates all major components of this strategy.

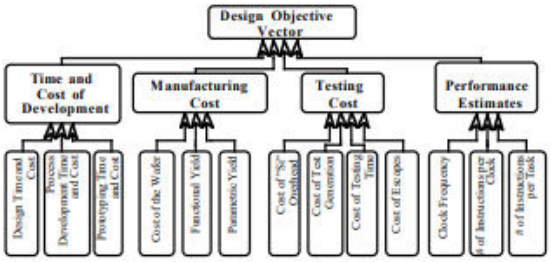

Fig 3 : *Cost models needed for system/IC level cost minimization purposes.*

V CONCLUSION

The purpose of this paper was to give an overview of the problems with silicon cost and to start a discussion about what might happen if the IC manufacturing facility grew dramatically as planned. According to the facts presented, changes in silicon cost may have a significant impact on the VLSI design domain. It will be necessary to refocus VLSI design, test, and CAD on cost-related issues as a result of this change. For example, tools for system-level design cost optimization, analytical (not accounting) cost models, and tools and strategies for identifying and then minimizing manufacturing costs (yield learning, process simplifications, etc.) will all need to be developed.

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